

# **JEDEC PUBLICATION**

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## **3D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions**

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## **3D CHIP STACK WITH THROUGH-SILICON VIAS (TSVS): IDENTIFYING, EVALUATING AND UNDERSTANDING RELIABILITY INTERACTIONS**

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### **Introduction**

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To increase device bandwidth, reduce power and shrink form factor, microelectronics manufacturers are implementing three dimensional (3D) chip stacking using through silicon vias (TSVs). Chip stacking with TSVs combines silicon and packaging technologies. As a result, these new structures have unique reliability requirements. This document is a guideline that describes how to evaluate the reliability of 3D TSV silicon assemblies.

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## **3D CHIP STACK WITH THROUGH-SILICON VIAS (TSVS): IDENTIFYING, EVALUATING AND UNDERSTANDING RELIABILITY INTERACTIONS**

(From JEDEC Board Ballot JCB-09-64, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

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### **1 Scope**

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This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests provide guidance for qualifying new and modified technology/process/product families, as well as individual solid state surface-mount products. This publication is intended as a guideline to describe the extension of the standard tests to three-dimensional (3D) chip structures that contain stacks of two or more chips that use through-silicon vias to connect from the front side to the back side of each chip. The main element of this extension is the addition of appropriate test structures to evaluate the reliability of the TSVs and other new features introduced in the fabrication of 3D products. This publication applies to vias-first process (TSV formation before completion of the silicon device fabrication), vias-middle (TSV formed in the BEOL or prior to the BEOL process), and a vias-last process (TSV formation after completion of the silicon device fabrication). Although 3D TSV test structures may not be a prerequisite for silicon chip qualification, they are necessary if those chips are intended for use in 3D products. If the effects of 3D TSVs on a device technology placed in a specific packaging scheme are not known, there could be reliability concerns for that component (packaged part) that are not evident with standard component level test structures. Therefore, it is recommended to include 3D TSV test structures and associated testing and failure analysis to determine if there are any adverse effects on the assembly due to packaging.

This publication covers only interaction between the 3D TSV component, the semiconductor package, and the semiconductor device. Interactions between the assembled component and a second level assembly are not covered. See JEP150 for information regarding assembled component reliability.

The reliability stress tests referred to in this document have been found capable of stimulating and precipitating failures in components in an accelerated manner, but they should not be used indiscriminately. Failures from each test should be examined for:

- a) potentially new and unique failure mechanisms
- b) situations where these tests/conditions may induce invalid or overstress failures.

In either case, the set of reliability requirements, tests, and/or conditions should be appropriately modified to properly include the new failure mechanisms and modes.

This document does not relieve the supplier of the responsibility to meet internal or customer-specified qualification programs.

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## 2 Terms and Definitions

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**3D chip stack:** Two or more chips vertically connected to form a unified electrical structure in a single package.

**assembled state (of a component):** The state of a component that has been attached to a second-level assembly.

**back-end-of-line (BEOL) (adj):** Pertaining to the portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

**back end of line (BEOL) (noun):** The portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

**bond and assembly process (B&A):** A process associated with connecting chips (dice) to other package elements and assembling semiconductor-device packages.

**chip stack:** A group of interconnected silicon chips stacked vertically to make a 3D structure.

**chip-to-chip interconnect; level D interconnect:** The structure that connects one chip in a 3D stack to another chip in that 3D stack.

NOTE Examples of this structure include, but are not limited to, solder bumps and copper pads.

**chip-to-package interaction (CPI):** For the purpose of this document, the interaction between stresses induced by the semiconductor package and the semiconductor chip whether alone or within the semiconductor 3D chip stack.

**chip-to-substrate-interconnect; level 1 (L1) interconnect:** The structure that connects a chip to a substrate.

NOTE 1 For the purpose of this document a “chip-to-substrate-interconnect” is referred to as an “interconnect”.

NOTE 2 Examples of this structure include, but are not limited to, solder bumps and copper columns.

NOTE 3 Level 1 (L1) interconnect is not associated with JP 001 Foundry Level 1 Qualification (L1).

**dice:** Plural of die.

**distance to neutral point (DNP):** The physical distance from the stress-neutral point to the point of interest on the die, chip stack, or interposer.



## 2 Terms and Definitions (cont'd)

**failure mechanism:** The physical, chemical, electrical, or other process that has led to a nonconformance.

NOTE 1 See JESD671, *Component Quality Problem Analysis and Corrective Action Requirements*.

NOTE 2 A failure mechanism may be characterized by how a degradation process proceeds including the driving force, e.g., oxidation, diffusion, electric field, current density.

**failure mode (general):** The way in which a failure mechanism manifests itself in a failing component.

NOTE Examples of failure modes are a visual blemish, a bent lead, a foreign particle or material, an incorrect dopant profile or grain size, a scratch, an electrical fault (open, short, leakage, inadequate slew rate or noise margin, stuck at high or low, etc.).

**far-back-end-of-line (FBEOL) (adj):** Pertaining to the portion of the semiconductor processing line that creates the metal layer (e.g., the UBM or redistribution layer) and associated interconnect structures forming the connection between on-chip and off-chip wiring.

**far back end of line (FBEOL) (noun):** The portion of the semiconductor processing line that creates the metal layer (e.g., the UBM or redistribution layer) and associated interconnect structures forming the connection between on-chip and off-chip wiring.

**free-standing state (of a component):** The state of a component that is not attached to the next level of assembly packaging.

**front-end-of-line (FEOL) (adj):** Pertaining to the portion of the semiconductor processing line that creates active devices, ending with the gate conductors.

**front end of line (FEOL) (noun):** The portion of the semiconductor processing line that creates active devices, ending with the gate conductors.

**packaged device:** A semiconductor device within an enclosure that allows electrical connection to, and provides mechanical and environmental protection for, that device.

**second-level assembly:** The attachment of a component to the next level of assembly packaging.

**stratum; tier:** Each individual layer of silicon in a chip stack.

**through-silicon via (TSV):** A conductive via that runs vertically through a silicon chip and electrically connects structures on the top side and the bottom side of the chip.

## 2 Terms and Definitions (cont'd)

**under-bump metal (UBM):** The metal layers located between the solder bump or column and the die.

NOTE This is also known as the bump-limiting metals (BLM).

**via-first:** A TSV formed before completion of the silicon device fabrication..

NOTE These vias may be created before or during front-end-of-line (FEOL) but before back-end-of-line (BEOL) processing. They are created by etching them from the top side of the wafer, and are buried below the subsequent BEOL layers. The process allows for interconnects with a high density. These vias connect circuits at the global or intermediate IC level.

**via-middle:** A TSV formed after FEOL processing and prior to or during the BEOL process.

NOTE A “via-middle” process is sometimes considered to be part of a “via-first” process.

**via-last:** A TSV formed after the completion of the silicon device fabrication, specifically after the completion of both FEOL and BEOL layer processes.

NOTE The TSVs connect circuits at the bond-pad level.

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## 3 References

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### 3.1 Informative references

JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*.

JEP131, *Process Failure Modes and Effect Analysis (FMEA)*.

JEP150, *Stress-test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components*.

JEP154, *Guideline for Characterizing Solder Bump Electromigration Under Constant Current and Temperature Stress*.

JEP156, *Chip Package Interaction Understanding, Identification and Evaluation Guideline*.

*Handbook of 3D Integration, Volume I and II*, P. Garrou, C. Bower and P. Ramm, Ed, Wiley-VCH.

### 3 References (cont'd)

#### 3.2 Normative references

JESD22, *Reliability Test Methods for Packaged Devices*.

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*.

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JESD85, *Methods for Calculating Failure Rate in Units of FITs*.

JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology*.

J-STD-020, *Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices*.

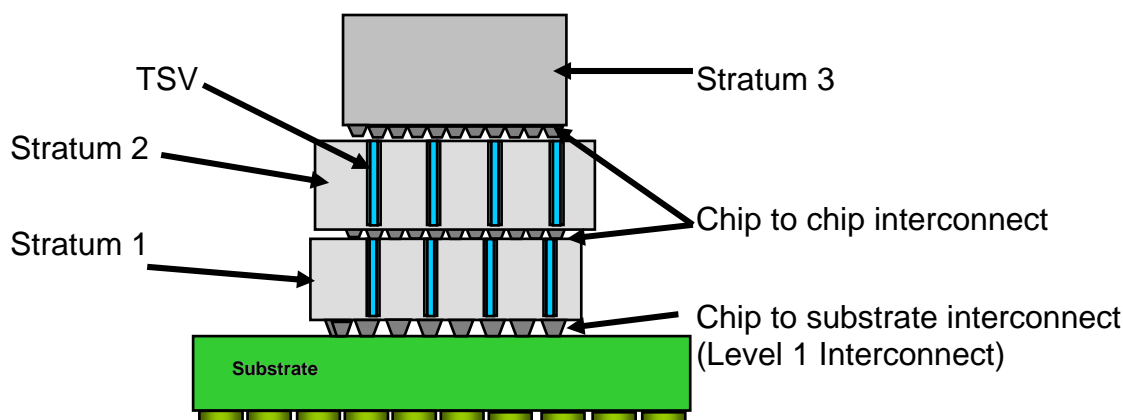
J-STD-033, *Joint IPC/JEDEC Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface-Mount Devices*.

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## 4 Overview of TSV Chip Stack Manufacturing and Reliability

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3D chip stacks are affected by the same stresses as single chips. However, in the 3D chip stack, there are extra silicon layers, called strata, and TSVs, which add more structures and complexity to the system (Figure 4-1 and Figure B-1). Instead of one plane of electrical inter-connections (from the chip to the package), there may be one or more additional planes of electrical inter-connections from one stratum in the stack to another stratum in the stack. The TSVs provide vertical intra-connections in through each stratum. Traditional CPI structures can be used to evaluate the inter-connections between strata in the 3D stack and between the chip stack and the package. New structures are used here to evaluate the TSV intra-connection.



**Figure 4-1 — 3D chip stack with TSVs and interconnections between strata in the stack**

## 4.1 TSV Formation

Typical processes associated with TSV formation include: (a) Via etch or drill, (b) Insulator/Diffusion Barrier/Seed Layer deposition and (c) Via fill.

Via formation is typically accomplished by etching a via a Deep Reactive Ion Etching (DRIE) process or by laser etching using UV lasers.

The insulator layer is generally a SiO<sub>2</sub> deposited by chemical vapor deposition (CVD). There are a few examples of using organic layers such as parylene, but few can be deposited conformally. This is followed by adhesion/diffusion barrier layer formation (typically Titanium Nitride). The next step is deposition of high quality seed layer to enable a continuous metallization in the through via. For copper TSVs, TiN and Cu seed layers are deposited by sputtering or other CVD techniques.

Via fill using Tungsten (W) is usually deposited by CVD processing. Copper metallization is done by electrochemical plating.

## 4.2 TSV Related Backside Processing

TSV related backside processing steps include thinning, etch-back, and passivation as well as redistribution layer. Many of these processes are unique to 3D chip stack and have associated reliability implications. The majority of 3D Chip stacking programs require TSV wafer thickness significantly below 100 µm. Handling of thin wafers, especially through the wafer backside processing steps require special technology. The TSV wafers are either mounted on temporary (handle) wafers, also called carrier wafers, or directly onto the 3D-IC chip stack, prior to thinning.

Structures to assess the impacts are sometimes better addressed during the process qualification through test vehicles or test chips. However, in certain cases, for example, impact of thinning may adversely affect certain specific transistor designs that need to be addressed at the product level. Thinning down to 25-50 µm may also lead to additional warpage related stress to devices. In addition, backside processing may lead to leakage to substrate as well as mobile ion diffusion.

TSV failure mechanisms will not appear in standard silicon chip stress testing due to the insensitivity of conventional single die test structures, even though the stress levels in the test may be much higher than those that can cause TSV fails. Mechanical stresses, which can scale with size, and defects introduced by the far back end of the wafer line and bond and assembly processes, can only be addressed through representative test structure design and processing, followed by stress testing and appropriate electrical and physical characterization (see 5).

### 4.3 3D Bond and Assembly

3D bond and assembly processes include chip to chip attachment, multiple chip attachment, chip reflow(s), underfill and cure, thermal enhancement apply, overmold or encapsulation apply, module test, burn-in, module card attach, and rework of any of these processes for flip chip plastic ball grid arrays (FCPBGA) and similar package types. The critical materials are:

- 1) the substrate,
- 2) interconnect,
- 3) chip-to-substrate underfill,
- 4) chip-to-chip underfill, and
- 5) thermal enhancement on the back of the chip (i.e., heat spreader, heatsink, package substrate or card).

### 4.4 Reliability Considerations for Various TSV Structures

TSVs can also affect the reliability of the usual Si structures. Stresses are generated in the Si by the presence of the TSV, due to the differences in CTE between the conductive material of the TSV and that of the Si, and due to the geometry of the TSV. Some field-effect transistors (FETs) are sensitive to stress, such that the FET electrical characteristics can vary with distance to a nearby TSV. These varying characteristics may also have an impact on conventional Si device wear out mechanisms. Where the TSV extends into the BEOL layers, imperfections in the TSV liner materials can lead to interfacial contamination of the dielectric layers, which may in turn lead to the eventual formation of leakage paths in wiring levels. The connection schemes between the TSVs and chip wiring provide additional opportunities for failure either by interfacial delamination or through electromigration due to current crowding caused by the juxtaposition of shapes with diverse dimensions. Also depending on the type of TSV, the processing needed to fabricate it, and the sequence of fabrication steps, thermal excursions can have deleterious effects on small wiring features and on features in low-k dielectrics. Thus an additional set of reliability structures are needed in the chip itself to focus specifically on the effect of the new features and processes on traditional chip wear out mechanisms. These structures will have different shapes and be tested somewhat differently, depending on whether the TSV is fabricated first (before the rest of the chip is built) or last (after the rest of the chip is built). In the case of TSV-first processes, the presence of the TSV and residual effects of TSV processing may influence subsequent processing and structures. In the case of TSV-last processes, the TSV fabrication steps can damage or alter existing structures already present in the chip. Different via processes can produce different aspect ratio TSVs. The aspect ratio will depend on the thickness of the wafer and the width or diameter of the TSV. Higher aspect ratio TSVs require more conformal deposition processes in order to not have incomplete film formation on the sidewall of the via. Higher aspect ratio vias also require better conductor fill in order to prevent voids or seams. Both incomplete fill formation on the sidewall and voids in the conductor can lead to reliability failures.

## 4.5 CPI Stresses

CPI stresses arise from the processes and materials used in attaching and encapsulating a chip forming a functional module. Thermal excursions, either alone, or in combination with mismatches in materials properties, such as the coefficient of thermal expansion (CTE), are a major source of mechanical stress on the chip. CTE stresses increase with increasing chip sizes. In addition, processing defects, such as dicing cracks or chip backside flaws, can serve as initiation points for CPI failure. Materials defects, such as particles in a thermal conduction adhesive, can serve as stress concentrators to promote CPI fails. Materials interactions, such as alloy or intermetallic formation, can cause volume changes that concentrate stress. Low-k dielectric materials in the chip are mechanically weak and tend to form weak interfaces with other materials. An improper cooling rate during chip attachment to the substrate can cause CPI failures. And non-uniform solder bump solidification, particularly on lead-free flip chip modules, can concentrate CTE stress. In 3D chip stacks, bond and assembly processes may be repeated as strata are added, and can increase thermal and / or mechanical defects. Additionally, the strata in a 3D stack are thinned to a thickness (typically  $< 100\ \mu\text{m}$ ) that is usually much less than that of a traditional silicon chip. As a result, thin strata may be more fragile and susceptible to cracking than full thickness chips. To see a few examples of potential CPI failures please refer to JEP156.

## 4.6 Hot Spot Thermal Issues

Thermal hot spots related to TSVs and/ or stacking and thinning can also create unique reliability issues. This is especially important for thin dice that are expected to carry high currents during operation. Structures (heaters/temperature sensors) should be used, especially during process characterization/qualification.

## 4.7 3D TSV Failure Modes

In addition to CPI failures, 3D chip stacks with TSVs can have bonding problems due to warping or non-uniformity. In the case where a stratum is very thin ( $< 100\ \mu\text{m}$ ), the die is less mechanically stable, and as a result, the die may warp as temperature is cycled. If the top or bottom surface of the thin die is not flat during bonding, the connection between the thin die and other strata in the stack or to the package may not occur as expected, leaving opens. Also, if a solder ball connection is used, the warping of the stratum may compress the molten solder, causing lateral expansion and unintentional bridging or electrical shorting of adjacent solder balls. Non-uniformity of the thin die is also a concern when metal to metal bonding is used to interconnect strata. In this case, if the metal pad height varies too much, incomplete or no bonding may occur leaving a highly resistive path or open.

TSVs can also be a source of a reliability failure. TSVs are electrical pathways that travel through the bulk silicon of a die. The conducting pathway is prevented from shorting to the bulk silicon by a surrounding insulator. Two types of defects can cause reliability fails in this system.

#### **4.7 3D TSV Failure Modes (cont'd)**

First, if the insulator surrounding the TSV is not continuous or has a defect, it can break down and allow leakage between the TSV conductor and the bulk silicon of the die. An electrical short between the TSV and ground could then lead to a functional anomaly. A second potential TSV problem is a void in the conductive material that makes up a via, or that connects to it. The void can grow over time and cause an open.

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### **5 TSV failure concerns and associated hardware design considerations**

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#### **5.1 Primary TSV reliability failure modes requiring evaluation**

TSVs connect both to other strata and to elements within a stratum. All of these interfaces may be somewhat different from standard packaging or chip fabrication processes and should be tested for reliability. All bonds between strata must be evaluated, especially those located at large distances-to-neutral points (DNP). These locations usually experience the greatest thermo-mechanical stresses due to CTE differences (both those between strata and those between different layers or structures within a stratum due to warpage), and can therefore suffer interfacial cracking and deformation of metallization layers in the connection scheme. The same interfaces are also vulnerable to electromigration failure, if not properly designed. TSVs can cause cracking in the Si stratum due to both geometric and CTE effects, and deficient dielectric separation between the TSV and the stratum Si can lead to electrical leakage and shorting. The integrity of all of these interfaces can be affected by the order of operations – that is, whether the TSV is fabricated before the rest of the chip (stratum) is built, during the sequence of steps used to build the rest of the chip, or after the chip is built.

Additionally, the choice of the TSV fill material can also affect the overall reliability due to CTE mismatch with the bulk silicon substrate.

#### **5.2 Test vehicle design considerations**

Use of a test vehicle is likely to be required since actual product is unlikely to have the electrical test sensitivity to adequately isolate or detect TSV concerns or failures in either the chips or in the 3D chip stack. Failure analysis of a test vehicle can be considerably easier than that of a product, if the test structure is properly designed. However, validation of results on actual product is also recommended.

#### **5.3 3D Chip Stack with TSV Test Structures**

Individual test structures should be placed at multiple locations across the chip, and in the case of chip reliability structures, at varying distances from TSVs. A list of potential failure modes, examples of basic 3D chip stack with TSV structure types, and stress tests that can be used to discover specific failure modes is given in Table 1. Other structures are possible based on experience and product design. The number of test structures used on a test die may be limited based on test capability and substrate wiring limitations.

## 6 3D chip stack with TSV test guidelines

### 6.1 3D package test regimen

Table 1 shows a number of 3D chip stack with-TSV structure types, the failure modes they are designed to detect, the reliability stress that should be used and the recommended method of detection. Other structures are possible based on the particular technology test needs.

**Table 1 — General CPI Structure Types and Associated Failure Mode**

3D Structure Type	Failure Mode	Reliability Stress	Detection Method
1. TSV Chains and Serpentes	Leakage to bulk silicon, Metal interface delam. Corrosion / extrusions, Delamination, cracks BEOL crack, BEOL interfacial delam., BEOL chain short	Moisture Preconditioning, Thermal Cycle, THB/ HAST, HTS	Opens and Shorts Testing  Acoustic microscopy
2. Corner Sensor	Interconnect resistance increase/ open, Chip corner crack, Corner delamination, Dicing related damage	Moisture Preconditioning Thermal Cycle	Electrical Test (opens), Acoustic microscopy, Optical inspection
3. Perimeter Lines	Dicing related damage, Edge/corner, Shifted perimeter line	Thermal Cycle, THB, uHAST, HTS	Electrical Test (opens), Acoustic microscopy, Optical inspection
4. Chip-to-chip interconnect stitch chains for mechanical evaluations	BEOL in-chip cracking, Bump resistance increase/ open, Bump/ final via defects, BLM undercut, Chip corner crack, Marginal contact to substrate	Moisture Preconditioning, Thermal Cycle, HTS, I/T-Stress	Electrical Test (opens), Acoustic microscopy
5. Chip-to-chip interconnect electromigration and stress migration structures incl. TSVs in the circuit	Interconnect and barrier degradation, Interface contamination or marginality, TSV integrity	EM Testing	Electrical Test (opens), X-section
6. Conventional Si device reliability structures varying distances from TSVs	Shifts in FET characteristics or wear out mechanisms; retention time loss in capacitive memory cells	FET characterization, gate oxide and trench dielectric stress, and hot carrier stresses	Electrical test data comparison with identical structures located far from TSVs
7. Conventional BEOL test structures for Stress Voiding (SV) and BEOL time dependent dielectric breakdown (TDDB)	Shifts in structure resistance or the occurrence of electrical opens; Leakage	Elevated temperature bake; TDDB test	Electrical data comparison with identical structures located far from TSVs
8. Thermal Structures	Investigate thermal hotspots	Temp exposure; operational testing	IR camera
9.ESD and Latchup (LU) Structures	Impact of wafer thinning, Investigate process induced charging due to backside RDL	LU performance comparison of thin vs. normal dice, TSV std. processing	Latch up testing at package level, Functional testing at package level
NOTE Table 1 is presented as a guideline and only covers package/stacked chip interaction. JEP150 or similar 2 <sup>nd</sup> level interaction qualification methodology must be considered to fully qualify components incorporating 3D chip stack technology.			



## **6.2 Test samples**

Test samples can be tested in either wafer or package format, dependent on the tests being performed. For these test samples in package format, preconditioning should be performed per JESD22-A113. Reflows should reflect the solder regimen being used in the actual application, and should include packages with maximum dimensions for that application. The JESD22-A113 procedure first requires that the moisture sensitivity level (MSL), per J-STD-020, be determined before starting the preconditioning sequence to establish which moisture soak condition is appropriate, i.e., likely to pass. The presence of multiple interfaces between silicon layers, in addition to traditional interfaces between silicon and packaging materials, significantly increases the potential complexity of determining MSL for a TSV device. Not only is failure more difficult to determine than in conventional devices, the susceptibility of devices to moisture induced delamination and/or cracking is increased due to the numerous interfaces.

### **6.2.1 Lot guidelines**

To assess manufacturing variability and its impact on reliability, the component test samples should be comprised of several wafer, bumping, substrate, and assembly lots to evaluate variability from the component qualification family. Refer to the specific qualification test method, such as JESD47 or JP001, for the recommended number of lots for that stress test. Other appropriate means may be used with justification.

### **6.2.2 Test hardware**

Test hardware should include the recommended structures discussed in clause 5. If this is not possible, employment of functional components may be acceptable and can provide insight into actual product performance. However, if improperly selected, functional device parameters can mask test failures if they are not sensitive enough to the failure mode. Thus the use of a test vehicle is the preferred method to detect 3D chip stack TSV reliability concerns. In general, the structures used for reliability investigations should be chosen according to the following criteria: 1- relevancy for the intended use, 2- ease of analysis and 3- dominant failure mechanism to be investigated under the planned stress condition.

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## **7      Stress test**

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### **7.1    Procedure**

Many chip-level test structures can be tested while still in wafer form provided the TSVs are included and wafer level testing is enabled. Other chip-level structures will only be testable after the chips are assembled into 3D stacks and accessed through package pins.

Once the test hardware is assembled and prepared for testing, appropriate test procedures should be followed for the stress test being performed. Test results can be acquired by both discrete interval measurements or by in-situ continuous monitoring. The measurement regimen should be determined based on product requirements and tester availability. Appropriate tester setups should be followed, with care taken to guarantee that the test interval, tester accuracy and tester setup meet appropriate industry standards. If in-situ continuous monitoring is not used, a test method capable of resolving a low resistance change in each test pattern is necessary, such as the four-point probe methodology. With in-situ interval testing, the resistance change criteria used can be critical in the timely discovery of test fails.

Failure criteria, test regimen and test duration need to be set to highlight the specific failure mode for the appropriate application requirements. Failure may be defined both in terms of electrical or mechanical failure, but mechanical failure is irrelevant unless it leads ultimately to electrical failure. Mechanical failure criteria typically involve use of acoustic microscopy (AM) to detect internal device cracks and/or delamination. Electrical failure criteria can be either an absolute value, based on actual product resistance sensitivity, or a representative change in measured electrical resistance representing a test failure in each test pattern, often set at an increase of 20%. Alternatively, electrical failure criteria can be an absolute value based on actual product resistance sensitivity. In either case, the electrical test should record the value of the resistance shift. If the test method selected is not capable of resolving this level of resistance shift then there is the likelihood that test failures will not be detected in a timely manner, thus affecting any failure models or statistics being formulated. If a bench top discrete measurement technique is used, the test interval readout schedule should be determined based on the failure mechanisms of interest. Generally readouts are made more often in the early portion of the reliability test sequence in order to capture early test fails or test setup problems.

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## **8      Failure analysis**

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Failure analysis is used to verify the location and mechanism of the failure. See Annex A for a list of failure mechanisms and contributing factors. The most important aspect of failure analysis is the verification of the failure location. Also it must be determined that any failure would be the type that is relevant to application conditions and situations. As such, it is important to isolate the failure and assure that it is associated with the component and not the test setup, including the tester, cabling or the PWB on which the component of interest may have been assembled. Care must be taken during failure analysis not to disturb the failure. In particular, if the component needs to be removed from a printed wiring board (PWB), extreme care must be taken. Non-destructive failure analysis tools can also be used. They include acoustic microscopy (AM), 2D and 3D x-ray, time domain reflectometry (TDR), and side view optical microscopy. The stacked die structure of TSV devices places particular challenges upon traditional AM and x-ray techniques; determining the failure location can be very difficult due to the multiplicity of silicon wafer interfaces. Common methods used in destructive failure analysis include, but are not limited to, cross section, dye penetrant, scanning electron microscopy (SEM) and energy dispersive x-ray (EDX).

Special techniques may need to be developed for metrology of TSV related failures as well as metrology for TSV depth and fill measurement, thin wafer edge inspection and other backside process defects.

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## **9      Documentation**

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In general, details of the evaluated product, test set-up, and results should be reported. The request for this information should be specified in the applicable procurement documentation. Because the materials and geometries of the device and package can affect the chip to package interaction, this information should also be included. Annex A is an example of suggested information that might be provided in a report or available on request.

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## **Annex A (informative) – Example of Report Information**

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### Materials and geometries:

#### Si Chip:

Silicon metallization: materials, thickness, and dimensions of all metal layers

Overall device thickness, length and width

For each UBM layer: material, thickness, and deposition technique

UBM size

Passivation or repassivation opening size (where UBM contacts silicon metallization)

Passivation/repassivation materials and thickness

Bump composition

Bump deposition method

Bump height, both non-reflowed and after attaching to substrate

Bump pitch

Backside surface finish (mirror, matte, roughness)

#### Substrate:

For each layer of substrate metallization: material, thickness, and deposition technique

Substrate pre-solder composition, thickness, and deposition method, if applicable

Substrate solder resist opening (if applicable)

Solder mask

Substrate metal pad size

Substrate material

Substrate internal metallization composition

Substrate thickness, width and length

Substrate flatness

#### Package:

Underfill material (if applicable)

Die attach adhesive (if applicable)

Overmold / Glob Top (if applicable)

Adhesives

Stack-level testing process

#### Lid / Heatsink (if applicable):

Mass/ weight

Material

Size (x, y, z)

Thermal interface material

Attach methodology

## **Annex A (informative) – Example of Report Information (cont'd)**

### First Level Assembly Processing:

- Fluxes
- Solders
- Cleaning fluids
- Reflow profile for die and BGA attach to substrate
- Cure profiles

### Second Level Assembly Details, if applicable

- Profile
- Solder
- Flux
- Cleaning
- PWB details, such as, thickness, layers and copper content

### Testing:

- Diagram of how package is daisy chained under test
- Method of measuring device / package temperature
- Test parameters (current, voltage, limits, etc,)
- Test structures under test

### Failure criteria

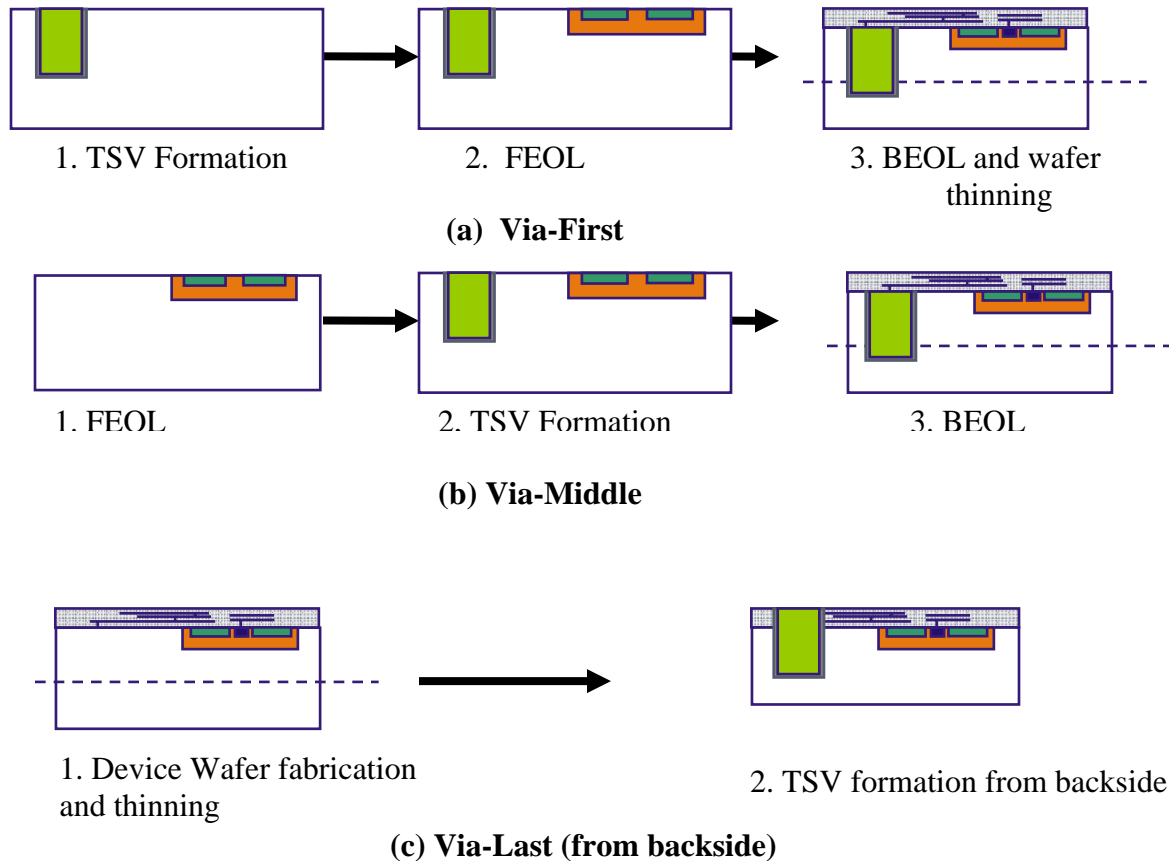
### Test chamber / procedure:

- Temperature variation across chamber
- Temperature profile
- Chamber start up procedure
- Initial device resistance at the stress condition (average and spread)
- Device current
- Chamber temperature / humidity
- Chamber loading
- Temperature rise of device due to Joule heating
- Device temperature
- Preconditioning details
- Sample size

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**Annex B (informative) Illustrations of Example TSV Construction Methods**


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NOTE 1 Examples of TSV fill material include doped polysilicon, W, and Cu.

NOTE 2 Another example of via-middle would include TSV formation within the overall BEOL processing.

NOTE 3 TSVs can be formed either from the front (e.g., Figure B-1a or Figure B-1b) or backside (e.g., Figure B-1c) of the wafer.

**Figure B-1 — Schematic of examples of (a) via-first, (b) via-middle and (c) via- last**



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## Standard Improvement Form

JEDEC JEP158

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The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC  
Attn: Publications Department  
3103 North 10<sup>th</sup> Street  
Suite 240 South  
Arlington, VA 22201-2107

Fax: 703.907.7583

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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Submitted by

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Date: \_\_\_\_\_

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